

## CLAIMS

We claim:

- 1           1. A chip scale package of an integrated circuit, comprising:  
2               (a) at least one solder ball pad; and  
3               (b) a moat around each solder ball pad.
  
- 1           2. The chip scale package of claim 1, in which at least one passivation layer is disposed on  
2 the integrated circuit, and in which the moat is formed in the at least one passivation layer.
  
- 1           3. The chip scale package of claim 2, in which the at least one passivation layer comprises a  
2 photo-imageable polymer film.
  
- 1           4. The chip scale package of claim 2, in which the at least one passivation layer has a  
2 thickness, and the moat is a full-depth moat having a thickness substantially equal to the thickness  
3 of the at least one passivation layer.
  
- 1           5. The chip scale package of claim 4, in which the at least one passivation layer comprises a  
2 photo-imageable polymer film.

1           6. The chip scale package of claim 2, in which the at least one passivation layer has a  
2 thickness, and the moat is a partial-depth moat having a thickness of approximately 1-99% of the  
3 thickness of the at least one passivation layer.

1           7. The chip scale package of claim 6, in which the at least one passivation layer comprises a  
2 photo-imageable polymer film.

1           8. The chip scale package of claim 1, in which a first passivation layer is disposed on the  
2 integrated circuit, and a second passivation layer, having a thickness, is disposed on the first  
3 passivation layer, and in which the moat is formed in the second passivation layer.

1           9. The chip scale package of claim 8, in which the moat is a full-depth moat having a moat  
2 depth substantially equal to the thickness of the second passivation layer.

1           10. The chip scale package of claim 9, in which at least the second passivation layer  
2 comprises a photo-imageable polymer film.

1           11. The chip scale package of claim 8, in which the moat is a partial-depth moat having a  
2 moat depth of approximately 1-99% the thickness of the second passivation layer.

1           12. The chip scale package of claim 11, in which at least the second passivation layer  
2 comprises a photo-imageable polymer film.

1           13. A wafer for a chip scale package, the wafer having at least one solder ball pad,  
2 comprising:

- 3           (a) a solder ball at each solder ball pad;  
4           (b) a polymer collar around the solder ball; and  
5           (c) a moat around each solder ball pad.

1           14. The wafer of claim 13, such that the moat prevents flow of liquefied polymer collar from  
2 within the moat to without the moat during and subsequent to heating of the wafer.

1           15. A method of manufacturing a wafer-level chip scale package, comprising the steps of:

- 2           (a) providing a wafer;  
3           (b) disposing a passivation layer on the wafer;  
4           (c) forming in the passivation layer a central feature for a solder ball; and  
5           (d) forming in the passivation layer a moat around the central feature.

1           16. The method of claim 15, including the steps of  
2           (e) placing a polymer collar within the moat; and  
3           (f) heating the wafer until at least some of the polymer collar liquefies, such that the  
4           moat prevents flow of liquefied polymer collar from within the moat to without the moat prior to,  
5           and during, curing of the liquid.

1           17. The method of claim 15, in which the moat is formed by a laser.

1           18. The method of claim 15, in which the moat is formed by a drill.

1           19. The method of claim 15, in which the passivation layer comprises a photo-imageable  
2           polymer film.

1           20. The method of claim 15, in which the moat is formed by photo-lithographic means.